AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for maintaining translation consistency in a computer which includes a ~~single~~ host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:

hardware means for providing an indication ~~indicating~~ whether a first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address, the at least one host instruction for execution by the host processor; and

software means for responding to the ~~an~~ indication and ~~that the memory address to be written stores the target instruction which has been translated to at least one host instruction~~ for assuring that the at least one host instruction ~~instructions translated from the target instructions stored at the memory address~~ will not be utilized once the first memory address has been written.

2. (Previously Presented) A system for maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer.

3. (Currently Amended) A system for maintaining translation consistency as claimed in Claim 1 in which the software means invalidates the at least one host instruction by marking the at least one host instruction at the second memory address ~~instructions translated from target instructions stored at the memory address~~.

4. (Canceled).

5. (Currently Amended) A system for maintaining translation consistency as claimed in Claim 1 in which the software means ~~for protecting against writing the memory address~~ removes the at least one host instruction from memory from the second memory address ~~translations associated with the memory address~~.

6. (Currently Amended) A system for maintaining translation consistency as claimed in Claim 1 in which the hardware means comprises:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and

a storage position in each storage location of the translation look aside buffer; and

in which the software means ~~for protecting against writing the memory address~~ removes the at least one host instruction from the second memory address ~~translations associated with the memory address~~.

7. (Currently Amended) A computer system comprising:

a ~~single~~ host processor designed to execute instructions of a host instruction ~~instructions~~ set,

software for translating instructions from a target instruction set to instructions of the host instruction set,

memory for storing target instructions from a program being translated,

a translation buffer for storing host instructions translated from target instructions for execution, and

hardware means for providing an indication whether a target memory address to be written stores a target instruction which has been translated to a host instruction that is stored at a host memory address and for generating an exception to a write access to the [[a]] target memory address ~~storing a target instruction which has been translated to a host instruction~~.

8. (Currently Amended) A computer system as claimed in Claim 7 in which the hardware means ~~for generating an exception~~ comprises a translation look-aside buffer including a plurality of storage locations for virtual and physical addresses of recently accessed memory, each of the storage locations also

including a storage position for indicating that an instruction at a respective target memory address has been translated to a host instruction.

9. (Currently Amended) A computer system as claimed in Claim 7 further comprising software means for responding to the ~~an~~ exception and ~~to a write access to a target address storing a target instruction which has been translated to a host instruction~~ for protecting against writing the target memory address until it has been assured that the host instruction ~~translations associated with the memory address~~ will not be utilized before being updated.

10-11. (Canceled).

12. (Currently Amended) A method of responding to an attempt to write a memory address including a target instruction which has been translated to a host instruction for execution by a computer system including a ~~single~~ host processor, the method including:

marking a memory address for ~~including~~ a target instruction which has been translated to a host instruction, the host instruction for execution by the host processor,

detecting ~~a memory address which has been marked when~~ an attempt ~~is made~~ to write to the memory address, and

responding to the detecting ~~detection of a memory address which has been marked~~ by protecting a target instruction at the memory address until it has

been assured that the host instruction ~~translations associated with the memory address~~ will not be utilized before being updated.

13-17. (Canceled).

18. (Currently Amended) A memory controller comprising:

an address translation buffer including a plurality of storage locations in which recently accessed virtual addresses are to be recorded and in which physical addresses represented by the virtual addresses are to be recorded,

each of the storage locations including means for indicating whether a physical address stores an instruction of a target instruction set which has been translated to an instruction of a host instruction set for execution by a computer system including a ~~single~~ host processor, the instruction of a host instruction set for execution by the memory controller; and

means for detecting an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the physical address.

19. (Currently Amended) A memory controller as claimed in Claim 18 in which the means for detecting ~~an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the address~~ comprises:

means for generating an exception in response to detection of the ~~an~~ indication, and

means for responding to the exception to indicate the [[a]] subsequent operation to be taken with respect to the ~~translated~~ instruction of a host instruction set before accessing the physical address.

20. (Currently Amended) A memory controller as claimed in Claim 18 in which the means for indicating comprises a storage position in the [[a]] storage location.